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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,176	02/26/2002	Toshitaka Hasegawa	826.1796	2408

21171 7590 11/06/2006

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,176	HASEGAWA, TOSHITAKA	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated September 29, 2006.

2. Claims 1-16 are presented for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 7-10, 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art from the original specification and drawings filed on February 26, 2002, hereinafter AAPA, in view of Morimoto, and Watts, US Patent 6336161.

5. In re claim 1, AAPA discloses a power supply control method in a system [fig.2] in which a power supply control device [e.g., 112, 122] is provided for each of a plurality of information processing devices [e.g., 111, 121] connected to a network, comprising:

- A representative information processing device [111] of the plurality of information processing devices issuing, according to a predetermined power-up/down schedule of said representative information processing device and other information processing devices, a power-up instruction to each power supply control device of the other information processing devices upon each activation [pg.7, ll.10-17].
- Instructing each of the other information processing devices to perform a power-down process [pg.7, ll.1-5].

6. AAPA did not disclose notifying each of the other information processing devices of a next power-up date and time, having each power supply control device enter a next power-up date and time and performing a power-up process when the entered power-up date and time comes; and did not disclose explicitly entering a next power-up date and time each time a power-down date and time comes [i.e., when to enter].

7. Morimoto discloses a power supply control method in a system [fig.17] in which a power supply control device [e.g., 112, 114] is provided for each of a plurality of information processing devices [e.g., 624, 625] connected to a network, comprising:

- A representative information processing device [600] of the plurality of information processing devices.
- Notifying each of the other information processing devices of a next power-up date and time and having each power supply control device enter a next power-up date and time [col.13, l.62 – col.14, l.22].
- Each power supply control device of said other information processing devices performing a power-up process when the entered power-up date and time comes [col.5, ll.18-24].

8. Watts discloses a power supply control method in a system [fig.1], comprising having each power supply control device enter system data [next power-up date and time] each time a power-down mode [date and time] comes [fig.2a].

9. It would have been obvious to one of ordinary skill in the art, having the teachings of AAPA, Morimoto and Watts before him at the time the invention was made, to modify the system taught by AAPA to include the teachings of Morimoto, as the distributed computing

architecture capable of preventing single point failure is well known and suitable for use with AAPA; and include the teachings Watts, as the saving of system data [e.g., next power-up date and time] prior to power-down to capture the most updated data is well known and suitable for use with AAPA. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to efficiently operate a system of a plurality of information processing devices [Morimoto: col.1, l.6 – col.2, l.11; distributed computing enables load balancing and other efficient operations] and safely restore the states of an information processing device after power-down [Watts: col.2, ll.38-49].

10. In re claim 2, AAPA, Morimoto and Watts disclose each and every limitation as discussed above in reference to claim 1. AAPA further discloses, issuing a power-down instruction to each of the other information processing device each time a power-down date and time comes [pg.7, ll.1-5].

11. As to claims 3-4 and 10, Morimoto discloses, wherein said power-up date and time given to each of said power supply control devices of said other information processing devices is obtained by any of said information processing devices or each of said other information processing devices adding an arbitrary margin to a power-up date and time in said predetermined power-up/down schedule [col.13, ll.50-54; arbitrary zero margin added to default].

12. As to claims 7-8 and 12, Morimoto discloses, wherein said power-up instruction or power-down instruction is sequentially issued at predetermined startup intervals [schedule] or power-down intervals [col.12, ll.11-21, ll.33-55].

13. In re claim 9, AAPA, Morimoto and Watts disclose each and every limitation as discussed above in reference to claim 1. AAPA, Morimoto and Watts disclose the method of operating the apparatus; therefore, AAPA, Morimoto and Watts disclose the apparatus.

14. In re claim 13, AAPA, Morimoto and Watts disclose each and every limitation as discussed above in reference to claim 1. AAPA, Morimoto and Watts disclose the method of operating the device; therefore, AAPA, Morimoto and Watts disclose the device.

15. In re claim 14, AAPA, Morimoto and Watts disclose each and every limitation as discussed above in reference to claim 1. AAPA, Morimoto and Watts disclose the method; therefore, AAPA, Morimoto and Watts disclose the program realizing the functions of the method.

16. In re claim 15, AAPA, Morimoto and Watts disclose each and every limitation as discussed above in reference to claim 1. Morimoto discloses receiving a computer program stored in a computer data signal embodied in a carrier wave to perform the method [col.4, ll.35-41].

17. Claims 5-6 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Morimoto and Watts as applied to claims 1, 2 and 9 above, and further in view of Sugahara et al., European Publication 0936532, hereinafter Sugahara.

18. AAPA, Morimoto and Watts disclose each and every limitation as discussed above. AAPA, Morimoto and Watts did not disclose a permission condition.

19. Sugahara discloses an information processing device which is a representative information processing device [31] in a plurality of information processing devices in a computer system [fig.1], comprising a power permission condition [status information] storage unit [44]

for storing a power permission condition of a predetermined current and other information processing devices [clients] and does not give the power instruction and the next power data and time before a power permission condition is satisfied although the power data and time comes [0046; issuance of power instruction at designated time is based on satisfying of conditions].

20. It would have been obvious to one of ordinary skill in the art, having the teachings of AAPA, Morimoto, Watts and Sugahara before him at the time the invention was made, to modify the information processing device taught by AAPA, Morimoto and Watts to include the teachings of Sugahara, in order to obtain the claimed information processing device and associated method. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to efficiently control power consumption [Sugahara: 0010].

21. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, in view of Morimoto, and Slaughter et al., US Patent 6014669, hereinafter Slaughter.

22. AAPA discloses a power supply control method for a plurality of information processing devices [e.g., 111, 121], comprising:

- Issuing, by one of said information processing devices [111], a power-up instruction to each of the information processing devices upon each activation [pg.7, ll.10-17].
- Instructing, by said one of said information processing devices, each of the other information processing devices to perform a power-down process [pg.7, ll.1-5].

23. AAPA did not disclose automatic power control at each of the other information processing devices.

24. Morimoto discloses a power supply control method in a system [fig.17] in which a power supply control device [e.g., 112, 114] is provided for each of a plurality of information processing devices [e.g., 624, 625] connected to a network, comprising:

- Notifying, by said one of said information processing devices [600], each of the information processing devices of a next power-up data and time [col.13, l.62 – col.14, l.22].
- Entering said next power-up date and time in each of the other information processing devices [col.13, l.62 – col.14, l.22].
- Performing a power-up process of each the other information processing devices when the next power-up date and time comes if no further power-up instruction has been received from said one of said information processing devices [col.5, ll.18-24].

25. It would have been obvious to one of ordinary skill in the art, having the teachings of AAPA, Morimoto and Slaughter before him at the time the invention was made, to modify the system taught by AAPA to include the teachings of Morimoto, as the distributed computing architecture capable of preventing single point failure [Slaughter: col.1, ll.41-54] is well known and suitable for use with AAPA. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to avoid single point failure.

Response to Arguments

26. Applicant's arguments filed September 29, 2006 have been fully considered but they are not persuasive.

27. Applicant argues that "AAPA cannot be a valid reference under the provisions of 102". Examiner disagrees as the labeling of figure 2 is clearly an admission that what is pictured is

prior art relative to applicant's improvement. Furthermore, "conventional" indicates an accepted standard that is already well known by others.

28. Applicant argues that Morimoto does not teach "notifying each of the other information processing devices of a next power-up data and time". Examiner disagrees and submits figure 17 clearly illustrates the representative information processing device [600] notifying the next power-up data and time [116] via 107.

29. Applicant argues that Watts does not teach "having each power supply control device enter a next power-up date and time each time a power-down data and time comes". Examiner submits that the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. As discussed, Morimoto teaches "notifying each of the other information processing devices of a next power-up data and time", but did not discuss the detail of when to enter the information of next power-up data and time. However, it is well known in the art that information should be saved in nonvolatile memory prior to power down in order to prevent data loss. Nevertheless, Examiner still provided Watts to teach entering information when a power-down data and time comes. Examiner fails to see why one with ordinary skill in the art would not enter the next power-up data and time when a power-down has come so that the information is not lost and the system can be powered up correctly and restored safely.

30. As such, Applicant's arguments are deemed not persuasive and the rejections are respectfully maintained.

Conclusion

31. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen
October 19, 2006

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
11/3/06